Intel® Xeon™ Processor and Intel® *E7500/E7501 Chipset Compatible Platform*

Design Guide Addendum for Embedded Applications

July 2003

Order Number: 273707-004

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Revision History

Date	Revision	Description
July 2003	-004	Updated memory interface routing information and added Low Voltage Intel® Xeon™ processor information.
January 2003	-003	Updated and expanded memory interface routing information. Added E7501 chipset information.
June 2002	-002	Document Update
January 2002	-001	Initial Release

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1.0 Introduction

This document is an addendum to the *Intel® Xeon™ Processor and Intel® E7500/E7501 Chipset Compatible Platform Design Guide*. It contains applied computing-specific guidelines, such as uni-processor design guidelines, angled Double Data Rate (DDR) guidelines and single channel DDR guidelines.

Carefully follow the design information and recommendations provided in this document. These design guidelines have been developed to ensure maximum flexibility for system designers while reducing the risk of board-related issues.

Note that the guidelines recommended in this document are based on experience and preliminary simulation work done at Intel.

1.1 Reference Documentation

Table 1. Reference Documents (Sheet 1 of 2)

Document	Location
Intel® E7501 Chipset Memory Controller Hub (MCH) Datasheet	http://developer.intel.com/design/chipsets/datashts/251927.htm
Intel® Xeon™ Processor and Intel® E7500/E7501 Chipset Compatible Platform Design Guide	http://developer.intel.com/design/chipsets/designex/251929.htm
Intel® Xeon™ Processor with 512 KB L2 Cache and Intel E7500 Chipset Platform Design Guide	http://developer.intel.com/design/chipsets/e7500/guides/298649.htm
Intel® Xeon™ Processor with 512 KB L2 Cache at 1.80 GHz to 2.40 GHz Datasheet	http://developer.intel.com/design/Xeon/datashts/298642.htm
Intel® E7500 Chipset Memory Controller Hub (MCH) Datasheet	http://developer.intel.com/design/chipsets/e7500/datashts/290730.htm
Intel® 82870P2 PCI/PCI-X 64-bit Hub 2 (P64H2) Datasheet	http://developer.intel.com/design/chipsets/e7500/datashts/290732.htm
Intel 82801CA I/O Controller Hub 3 (ICH-3) Datasheet	http://developer.intel.com/design/chipsets/e7500/datashts/290733.htm
Intel® 82870P2 PCI/PCI-X 64-bit Hub 2 (P64H2) Specification Update	http://www.intel.com/design/chipsets/e7500/specupdt/290735.htm
Intel® 82801CA I/O Controller Hub 3 (ICH3-S) Specification Update	http://www.intel.com/design/chipsets/e7500/specupdt/290739.htm
603-Pin Socket Design Guidelines	http://developer.intel.com/design/Xeon/guides/249672.htm
VRM 9.1 DC-DC Converter Design Guidelines	http://developer.intel.com/design/Xeon/guides/298646.htm
Intel® Xeon™ Processor Voltage Regulator Down (VRD) Design Guidelines	http://developer.intel.com/design/Xeon/guides/298644.htm
Intel® Xeon™ Processor with 512 KB L2 Cache System Compatibility Guidelines	http://developer.intel.com/design/Xeon/guides/298645.htm
Intel® Xeon™ Processor Thermal Design Guidelines	http://developer.intel.com/design/Xeon/guides/298348.htm
Intel® E7500 Chipset Thermal and Mechanical Design Guidelines	http://developer.intel.com/design/chipsets/e7500/guides/298647.htm

Table 1. Reference Documents (Sheet 2 of 2)

Document	Location
Intel® Xeon™ Processor Thermal Solution Functional Specifications	http://developer.intel.com/design/Xeon/applnots/249673.htm
Intel® Xeon™ Processor with 512 KB L2 Cache Thermal Models	http://developer.intel.com/design/Xeon/devtools/
Intel® Xeon™ Processor with 512 KB L2 Cache Mechanical Model in IGES	http://developer.intel.com/design/Xeon/devtools/
Intel® Xeon™ Processor with 512 KB L2 Cache Mechanical Model in ProE* Format	http://developer.intel.com/design/Xeon/devtools/
AP-728 Intel ® ICH Family Real Time Clock (RTC) Accuracy and Considerations Under Test Conditions	http://developer.intel.com/design/chipsets/applnots/292276.htm
ITP700 Debug Port Design Guide	http://developer.intel.com/design/Xeon/guides/249679.htm
Intel® Xeon™ Processor with 512 KB L2 Cache Signal Integrity Models	http://developer.intel.com/design/Xeon/devtools
PCI Bus Power Management Interface Specification, Revision 1.1	http://www.pcisig.com/specifications/conventional/pci_bus_power_management_interface
PCI Hot Plug Specification, Revision 1.1	http://www.pcisig.com/specifications/conventional/pci_hot_plug
PCI Local Bus Specification, Revision 2.2	http://www.pcisig.com/specifications/conventional/conventional_pci
PCI-PCI Bridge Architecture Specification, Revision 1.1	http://www.pcisig.com/specifications/conventional/pci_to_pci_bridge_architecture
PCI Standard Hot-Plug Controller and Subsystem Specification, Revision 1.0	http://www.pcisig.com/specifications/conventional/pci_hot_plug
PCI-X Specification, Revision 1.0a	http://www.pcisig.com/specifications/pcix_20/pci_x/
System Management Bus Specification (SMBus), Revision 1.1	http://www.sbs-forum.org/
Universal Serial Bus Specification, Revision 1.1	http://www.usb.org/developers/docs/
Low Voltage Intel® Xeon™ processor at 1.6 GHz and 2.0 GHz Datasheet	http://www.intel.com/design/intarch/datashts/273766.htm
Intel® Xeon™ processor with 533 MHz System Bus at 2.0 GHz to 2.8 GHz Datasheet	http://www.intel.com/design/xeon/datashts/252135.htm
Low Voltage Intel® Xeon™ processor for Embedded Applications Thermal Design Guidelines	http://www.intel.com/design/intarch/designgd/273764.htm

2.0 Uni-processor System Bus Routing Guidelines

This section covers the system bus source synchronous (data, address, and associated strobes) and common clock signal routing for Intel® Xeon™ processor with 512 KB L2 cache (400/533 MHz FSB)/Low Voltage Intel® Xeon™ processor (400 MHz FSB) and Intel® E7500/E7501 chipset-based systems, in a uni-processor (UP) configuration. Table 2 lists the signals and their corresponding signal types.

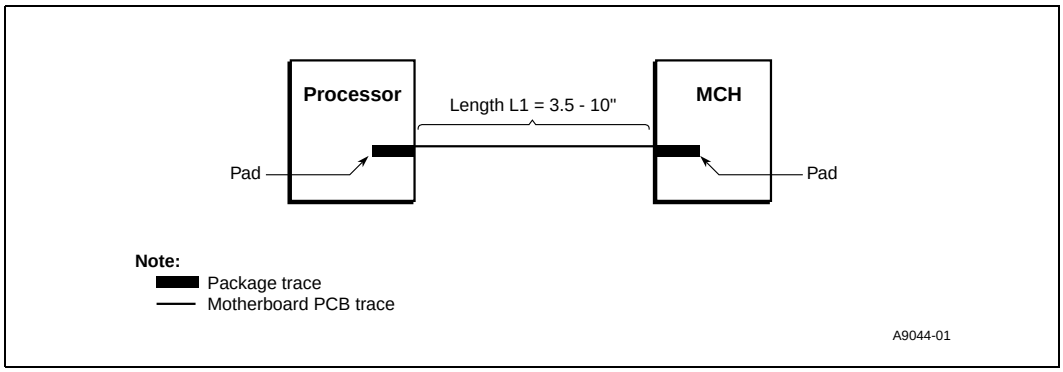
Figure 1 describes the uni-processor system bus topology.

Table 2. System Bus Signal Groups

Signal Group	Type	Signals
AGTL+ Common Clock Input	Synchronous to BCLK	BPRI#, BR[3:1]#[1,2], DEFER#, RESET#[1], RS[2:0]#, RSP#, TRDY#
AGTL+ Common Clock I/O	Synchronous to BCLK	ADS#, AP[1:0]#, BINIT#[3], BNR#[3], BPM[5:0]#[1], BR0#[1], DBSY#, DP[3:0]#, DRDY#, HIT#[3], HITM#[3], LOCK#, MCERR#[3]
AGTL+ Source Synchronous I/O: 4X Group	Synchronous to associated strobe	D[63:0]#, DBI[3:0]#
AGTL+ Source Synchronous I/O: 2X Group	Synchronous to associated strobe	A[35:3]#[4], REQ[4:0]#
AGTL+ Strobes	Synchronous to BCLK [1:0]	ADSTB[1:0]#, DSTBN[3:0]#, DSTBP[3:0]#
Async GTL+ Input[1]	Asynchronous	A20M#, IGNNE#, INIT#[4], LINT0/INTR, LINT1/ NMI, PWRGOOD, SMI#[4], SLP#, STPCLK#
Async GTL+ Output[1]	Asynchronous	FERR#, IERR#, THERMTRIP#, PROCHOT#[7]
System Bus Clock	Clock	BCLK0, BCLK1
TAP Input[6]	Synchronous to TCK	TCK, TDI, TMS, TRST#
TAP Output[6]	Synchronous to TCK	TDO
SMBus Interface[1]	Synchronous to SM_CLK	SM_EP_A[2:0], SM_TS_A[1:0], SM_DAT, SM_CLK, SM_ALERT#, SM_WP
Power/Other	Power/Other	GTLREF[3:0], COMP[1:0], OTDEN, RESERVED, SKTOCC#, TESTHI[6:0], VID[4:0], VCC_CPU, SM_V_{CC}[5], V_{CCA}, V_{SSA}, $V_{CCIOPLL}$, V_{SS}, $V_{CCSENSE}$, $V_{SSSENSE}$

NOTES:
1. These signals do not have on-die termination on the processor. They must be terminated properly on the system board. If the signal is not connected, it must be pulled to the appropriate voltage level through a 1 kΩ ± 5% resistor.
2. Xeon processors use only BR0# and BR1#.
3. These signals are 'wired-OR' signals and may be driven simultaneously by multiple agents. For further details on how to implement wired-OR signals, refer to the routing guidelines in Section 2.2.1.
4. The value of these pins driving the active edge of RESET# determine processor configuration options.
5. SM_V_{CC} has critical power sequencing requirements.
6. Terminations and routing for TAP signals and all debug port signals are found in the *ITP700 Debug Port Design Guide*.
7. PROCHOT# is input/output on Low Voltage Intel® Xeon™ processor D-stepping and beyond.

Figure 1. Uni-processor System Bus Topology



Refer to Table 3 for a summary of the uni-processor system bus routing recommendations. Use this as a quick reference only. The following sections provide more information for each parameter. Intel strongly recommends simulation of all signals to ensure that setup and hold times are met.

Table 3. Uni-processor System Bus Routing Summary

Parameter	Platform Routing Guidelines
Trace width/spacing	5/15 mils
4X signal group line lengths	3.5“– 10“pin-to-pin Length must be added to the system board trace between agents to compensate for the stub created by the processor package
DSTBn/p[3:0]# line lengths	DSTB# signals should follow the same routing rules as the data signals A 25 mil spacing should be maintained around each strobe signal (between DSTBp# and DSTBn#, and any other signal.)
2X signal group line lengths	Address signals should follow the same routing rules as the data signals.
ADSTB[1:0]# line lengths	ADSTB# signals should follow the same routing rules as the DSTB# signals.
Common clock signal line lengths	Common clock signals should follow the same routing rules as the data signals, however no length compensation is necessary.
Topology	The processor must have on-die termination enabled.
Routing priorities	All signals within the same strobe group must be routed on same layer for the entire length of the bus.
Reference plane requirements	Ground reference only. Avoid changing layers when routing system bus signals. If a layer change must occur, use vias connecting the two reference planes to provide a low impedance path for the return current. Vias should be as close as possible to the signal via.
System board Impedance	50 Ω ± 10%

2.1 Routing Guidelines for the 2X and 4X Signal Groups

The 4X group of signals uses four times the frequency of the base clock, or 400 MHz. The 2X group uses twice the frequency of the base clock, or 200 MHz. The 2X and 4X signals are listed in Table 4. Table 5 lists the 2X and 4X signals with their associated strobes.

Table 4. 2X and 4X Signal Groups

2X Group	4X Group
HA[35:3]# REQ[4:0]#	HD[63:0]# DBI[3:0]#

Table 5. Source Synchronous Signals and Associated Strobes

Signals	Associated Strobe
REQ[4:0]#, HA[16:3]#	ADSTB0#
HA[35:17]#	ADSTB1#
HD[15:0]#, DBI0#	DSTBP0#, DSTBN0#
HD[31:16]#, DBI1#	DSTBP1#, DSTBN1#
HD[47:32]#, DBI2#	DSTBP2#, DSTBN2#
HD[63:48]#, DBI3#	DSTBP3#, DSTBN3#

Routing guidelines for the 2X and 4X signal groups are given below:

- Trace impedance = 50 Ω ± 10%
- Route traces using 5/15 mil spacing
- Route all traces at least 25 mils away from the strobes
- Route all traces with at least 50% of the trace width directly over the reference plane for short distances only when needed in the interposer socket region.
- Route signals and their associated strobes on the same layer for the entire length of the bus.
- A strobe and its complement must be routed within 25 mils of the same length over the entire length of the buses.
- All 2X and 4X signals of the same group (refer to Table 5) must be routed within ±25 mils of the same length between the agents and within ±50 mils of the entire length of the bus.
- Total bus length must not exceed 10”.
- Trace length matching is required. Please contact your Intel field representative for a length matching spreadsheet.

Trace length matching is required within each source synchronous group to compensate for the package trace length differences between data signals and the associated strobe. This will balance the strobe-to-signal skew in the middle of the setup and hold window. Figure 1 shows how to implement trace length matching. An example of trace length matching is given in Equation 1.

2.1.1 Design Recommendations

Below are the design recommendations for the data, address, strobes, and common clock signals. For the following discussion, the pad is defined as the attach point of the silicon pad to the package substrate.

DATA:

- The pin to pin distance from the processor to the chipset should be between 3.5" to 10" (i.e., 3.5" < L1 < 10"). Data signals of the same source synchronous group should be routed to the same pad to pad length within ± 100 mils of the associated strobes. As a result, additional traces will be added to some data nets on the system board in order for all trace lengths within the same data group to be the same length (± 100 mils) from the pad of the processor to the pad of the chipset. This length compensation will result in minimizing the source synchronous skew that exists on the system bus. Without the length compensation the flight times between a data signal and its strobe is different, which results in an inequity between the setup and hold times.

Equation 1. Calculating Package Delta Addition to System Board Length for UP Systems

$$delta_{net,strobe} = (cpu\_pkglen_{net} - cpu\_pkglen_{strobe\dagger}) + (chipset\_pkglen_{net} - chipset\_pkglen_{strobe})$$

† Strobe package length is the average of the strobe pair.

ADDRESS:

- Address signals follow the same rules as data signals except they should be routed to the same pad to pad length within ±200 mils of the associated strobes. Address signals may change layers if the reference plane remains Vss and as long as the layers for a given group are all of the same configuration (all stripline or all microstrip).

STROBE:

- A strobe and its complement should be routed to a length equal to their corresponding data group's median pad-to-pad length ±25 mils. This causes the strobe to be received closer to the center of the data pulse, which results in reasonably comparable setup and hold times. A strobe and its complement (xSTBp/n#) should be routed to ±25 mils of the same length. It is recommended to simulate skew in order to determine the length that best centers the strobe for a given system.

COMMON CLOCK:

- Common clock signals should be routed to a minimum pin-to-pin system board length of 6" and a maximum motherboard length of 10".

2.2 Routing Guidelines for Common Clock Signals

Table 6 lists the common clock signals.

Table 6. Common Clock Signals

Signal Type	Signals
AGTL+ Common Clock Input	BPRI# BR[3:1]# DEFER# RESET# RS[2:0]# RSP# TRDY#
AGTL+ Common Clock I/O	ADS# AP[1:0]# BINIT# BNR# BPM[5:0]# BR0# DBSY# DP[3:0]# DRDY# HIT# HITM# LOCK# MCERR#

Routing guidelines for the source synchronous signal group are given below:

- Trace impedance = 50 Ω ±10%
- Route traces using 5/15 mil spacing
- Keep signals on the same layer for the entire length of the bus
- Route traces with at least 50% of the trace width directly over a reference plane
- Total bus length must not exceed 10"

2.2.1 Wired-OR Signals

There are five wired-OR signals on the system bus. These signals are HIT#, HITM#, MCERR#, BINIT#, and BNR#. These signals differ from the other front-side bus signals in that more than one agent can be driving the signal at the same time. Timing and signal integrity must be met for the case where one agent is driving, all agents are driving, or any combination of agents are driving.

The wired-OR signals should follow the same routing rules as the common clock signals. Intel recommends that simulations for these signals be performed for a given system.

2.3 Routing Guidelines for Asynchronous GTL+ and Miscellaneous Signals

This section provides routing guidelines for the signals listed in Table 7.

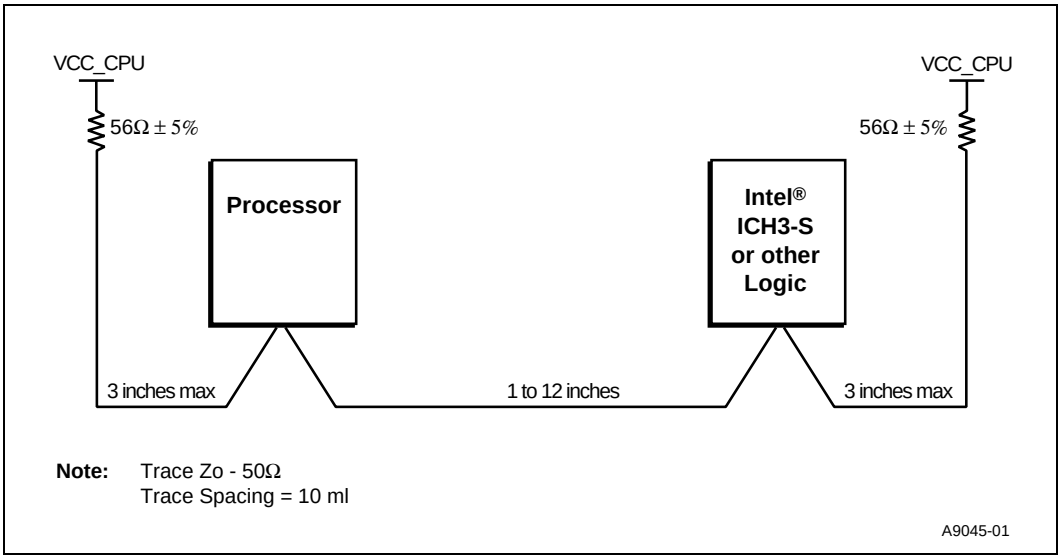
Table 7. Asynchronous GTL+ and Miscellaneous Signals

Signal Name	Type	CPU I/O Type	Driven by	Received by
A20M#	Async GTL+	I	ICH3-S	Processor
BINIT#	AGTL+	I/O	Processor	Processor
BR[3:1]#	AGTL+	I	Processor	Processor
BR0#	AGTL+	I/O	Processor/MCH	Processor/Chipset
COMP[1:0]	Analog	I	Pull-down	Processor
FERR#	Async GTL+	O	Processor	Chipset
IERR#	Async GTL+	O	Processor	External Logic
IGNNE#	Async GTL+	I	ICH3-S	Processor
INIT#	Async GTL+	I	ICH3-S	Processor
LINT[1:0]	Async GTL+	I	ICH3-S	Processor
ODTEN	Other	I	Pull-up/Pull-down	Processor
PROCHOT#	Async GTL+	O	Processor	External Logic
PWRGOOD	Async GTL+	I	External Logic	Processor
SLP#	Async GTL+	I	ICH3-S	Processor
SM_ALERT#	SMBUS (3.3 V)	O	Processor/Controller	Controller
SM_CLK	SMBUS (3.3 V)	I/O	Processor/Controller	Processor/Controller
SM_DAT	SMBUS (3.3 V)	I/O	Processor/Controller	Processor/Controller
SM_EP_A[2:0]	SMBUS (3.3 V)	I	Pull-up/Pull-down	Processor
SM_TS_A[1:0]	SMBUS (3.3 V)	I	Pull-up/Pull-down	Processor
SM_WP	SMBUS (3.3 V)	I	External Logic	Processor
SMI#	Async GTL+	I	ICH3-S	Processor
STPCLK#	Async GTL+	I	ICH3-S	Processor
THERMTRIP#	Async GTL+	O	Processor	External Logic
VCCA	Power	I	Pull-up/Pull-down	Processor
VCCIOPLL	Power	I	Pull-up/Pull-down	Processor
VCCSENSE	Other	O	Processor	Voltage Regulator
VID[4:0]	Other	O	Processor	Voltage Regulator
GTLREF	Power	I	Pull-up/Pull-down	Processor
VSSA	Power	I	Pull-up/Pull-down	Processor

2.3.1 Asynchronous GTL+ Signals Driven by the Processor

Follow the topology shown in Figure 2 when routing FERR#, IERR#, PROCHOT# and THERMTRIP#. Note that FERR# is the only signal in this group that connects the processors to the ICH3-S. IERR#, PROCHOT# and THERMTRIP# connect to other motherboard logic (such as the Baseboard Management Controller) and may need voltage translation logic, depending on the motherboard receiver logic devices used. Do not route a stub when routing to the processors.

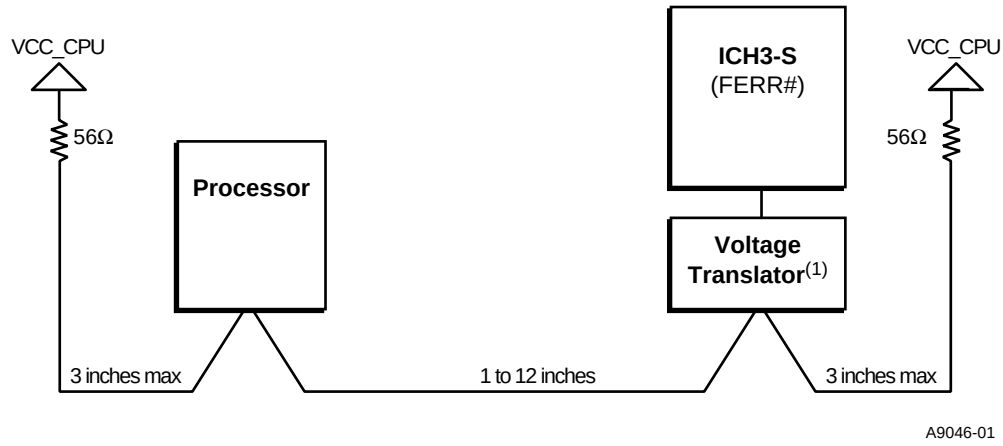
Figure 2. Topology for Asynchronous GTL+ Signals Driven by the Processor



2.3.1.1 Voltage Translation for FERR#

A voltage translator circuit is required for the FERR# signal when VCC_CPU is less than 1.3 V, as it is for the Low Voltage Intel® Xeon™ Processor. The required routing topology for FERR# is given in Figure 3. Figure 6 shows the voltage translator circuit.

Figure 3. FERR# Routing Topology for Low Voltage Intel® Xeon™ Processors

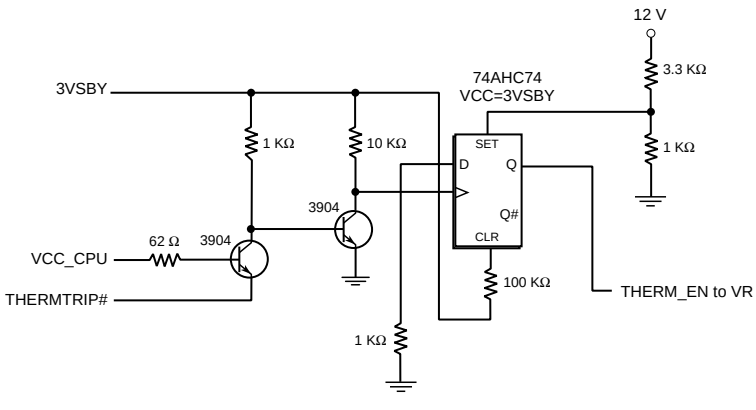


NOTE:
1. Refer to Figure 6 for voltage translator information.

2.3.1.2 Proper THERMTRIP# Usage

To protect the processors from damage in over-temperature situations, power to the processor core must be removed within 0.5 seconds of the assertion of the THERMTRIP#. If power is applied to a processor when no thermal solution is attached, normal leaking currents causes the die temperature to rapidly rise to levels at which permanent silicon damage is possible. This high temperature causes THERMTRIP# to go active. Use dual termination on the THERMTRIP# signal. Each processor's THERMTRIP# can be routed to its own receiver, or they can be wire-OR'd together. If routed separately, each signal must be terminated at the receiver end only. All power supply sources to all processors must be disabled when any install processor signals THERMTRIP#. In the reference schematic, the 74AHC74 flip-flop latches the THERMTRIP# signal HIGH after a PWRGOOD assertion, and LOW after a THERMTRIP# assertion. The recommended THERMTRIP# circuit is shown in Figure 1.

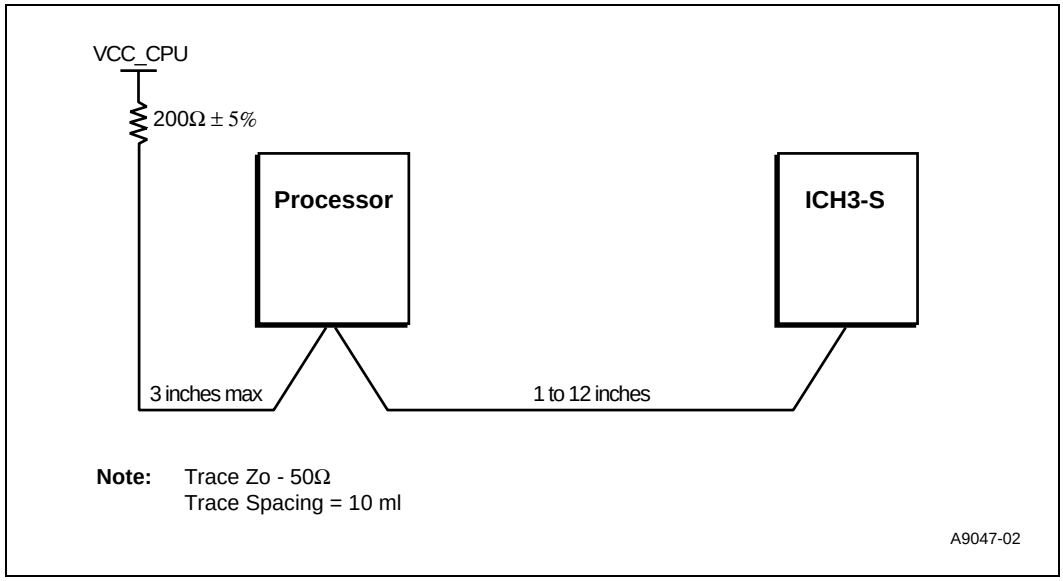
Figure 1. Recommended THERMTRIP# Circuit



2.3.2 Asynchronous GTL+ Signals Driven by the Chipset

Follow the topology shown in Figure 4 when routing A20M#, IGNNE#, INIT#, NMI, INTR, CPUSLP#, SMI#, STPCLK#, LINIT[1:0] and PWRGOOD.

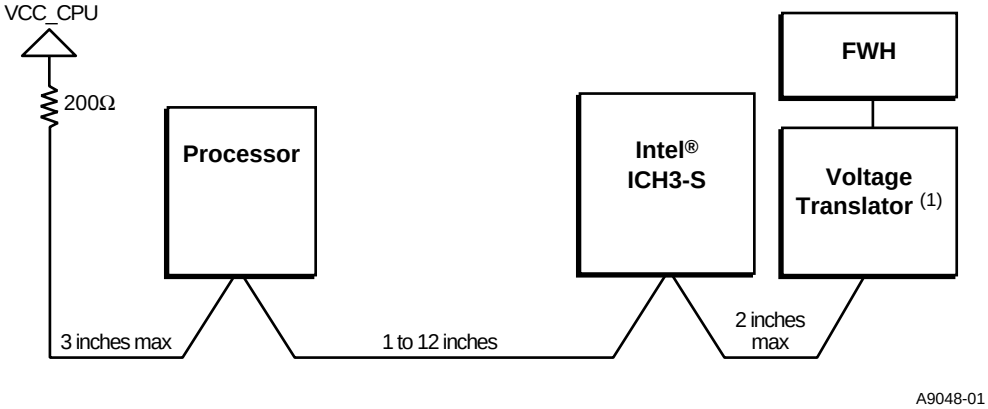
Figure 4. Topology for Asynchronous GTL+ Signals Driven by the Chipset



2.3.2.1 Voltage Translation for INIT#

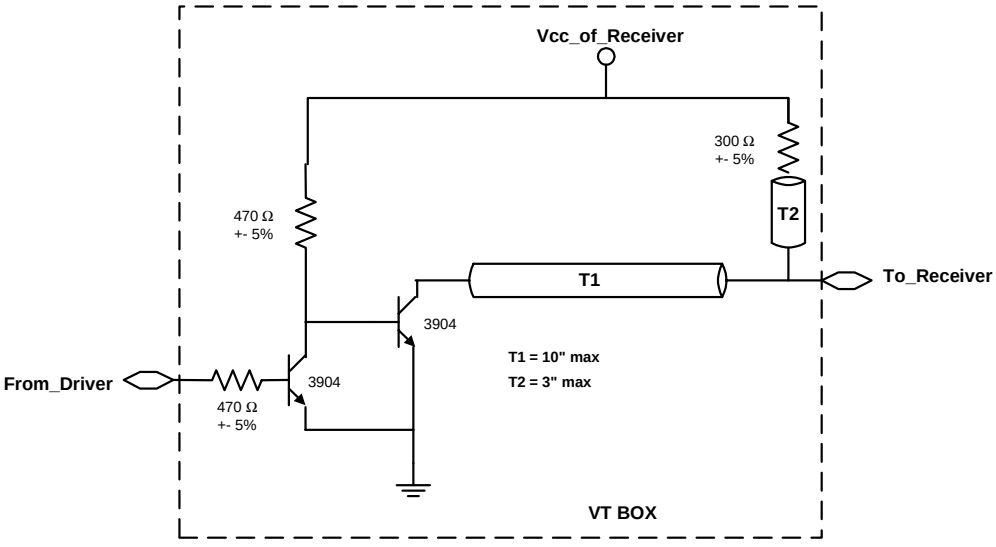
A voltage translator circuit is required for the INIT# signal for all platforms that use FWH. The required routing topology for INIT# is given in Figure 5. Do not route a stub when routing to the processors. Figure 6 shows the voltage translator circuit.

Figure 5. INIT# Routing Topology for a Uni-processor System



NOTE: 1. Refer to Figure 6 for voltage translator information.

Figure 6. Voltage Translator Circuit



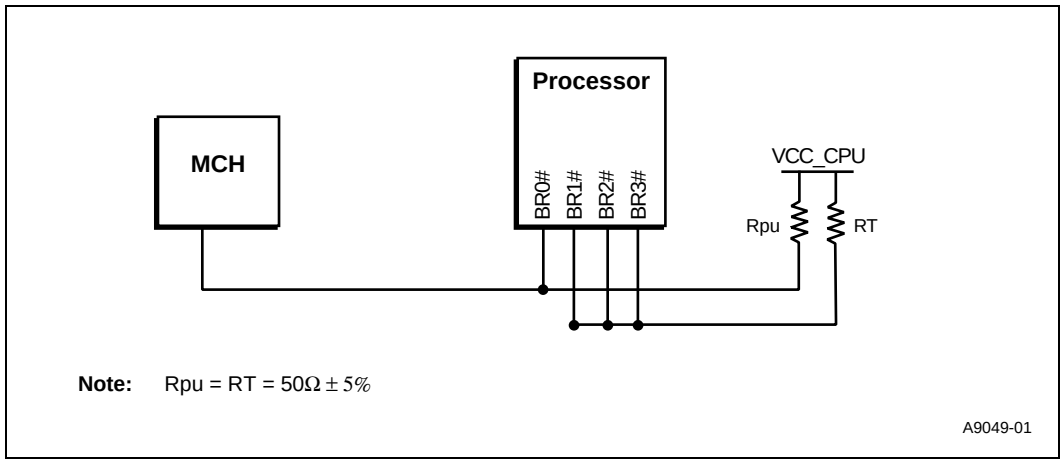
Note: T1 and T2 must be referenced to ground

2.3.3 BR[3:0] Routing Guidelines for Uni-processor Designs

Connect BR[3:0] as shown in Figure 7. The total bus length must be less than 10". The agent-to-Rpu stub must be 1" or shorter.

Note: BR3#, BR2# and BR1# are not used and pulled to VCC_CPU.

Figure 7. BR[3:0]# Connection for UP Configuration



3.0 Memory Interface Routing Guidelines

This section documents the configurations Intel simulated to support the memory routing guidelines detailed in the following sections. The customer should simulate any deviations from these recommendations.

The Intel® E7501 chipset may operate in a dual or single DDR channel configuration in DDR200 mode. These configurations are defined as follows:

- Dual channel configuration: The MCH consist of two DDR memory channels, channels A and B, that operate in ‘lock-step’. Each channel consists of 64 data and eight ECC bits. Logically, this is one, 144-bit wide memory bus; however, each channel is separate electrically. Intel® E7500 supports only dual channel.
- Single channel configuration: The MCH consists of one DDR memory channel, channel A. The channel consists of 64 data and 8 ECC bits.

To differentiate between dual and single channel requirements this section is divided into two subsections:

- Section 3.2, “Dual Channel DDR Overview” describes the requirements for a dual channel configuration.
- Section 3.3, “Single Channel DDR Overview” describes the requirements for a single channel configuration.

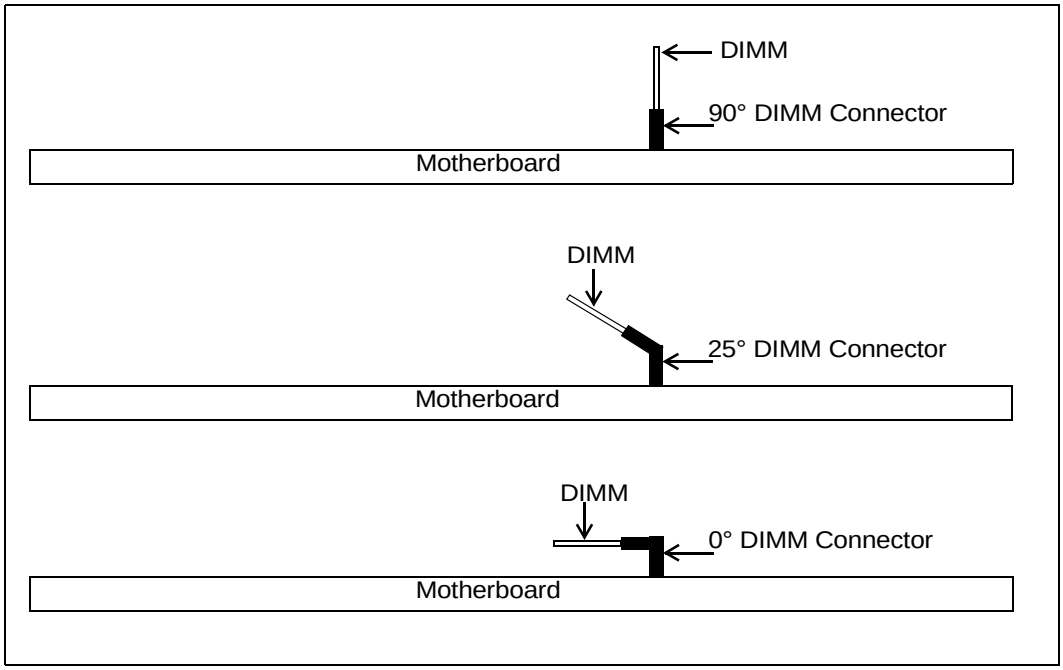
Each section covers its associated routing guidelines for the memory interface. Note that these guidelines apply to channel A and channel B for dual channel operation or channel A for single channel operation.

Refer to the *Intel® E7501 Chipset Memory Controller Hub (MCH) Datasheet* (order number 251927) for details on the signals.

3.1 DIMM Types

To allow flexibility in platform design this design guide supports three different DIMM connector types: 0-degree, 25-degree and 90-degree (see Figure 8). Routing guidelines are provided for each DIMM connector type in the following sections.

Figure 8. DIMM Connector Styles Supported



3.2 Dual Channel DDR Overview

In a dual channel DDR configuration, channel A and B are active and operate in lock-step which logically appears to be one 144-bit wide memory bus; however, each channel is separate electrically. Figure 9 and Figure 10 show both channels being routed to a single bank of DIMMs. The letters ‘A’ and ‘B’ in the DIMM figure refer to the DIMM channel. The number following ‘A’ or ‘B’ refers to the DIMM logical group. The DIMMs are physically interleaved. Intel recommends using this ordering, starting with Channel B closest to the MCH, for optimal routing.

The platform requires DDR DIMMs to be populated in-order, starting with the two DIMMs furthest from the MCH in a ‘fill-farthest’ approach (see Figure 10). This recommendation is based on the signal integrity requirements of the DDR interface. Intel’s recommendation is to check for correct DIMM placement during BIOS initialization. Additionally, it is strongly recommended that all designs follow the DIMM ordering, SMBus Addressing, Command Clock routing and Chip Select routing documented in Figure 9 and Figure 10. This addressing must be maintained to be compliant with the reference BIOS code supplied by Intel.

Figure 9. 1-DIMM per Channel Implementation

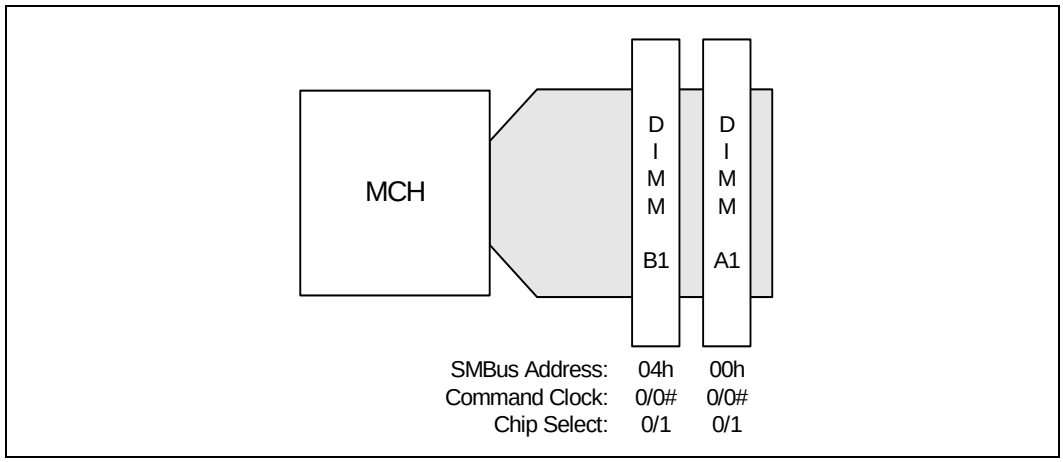
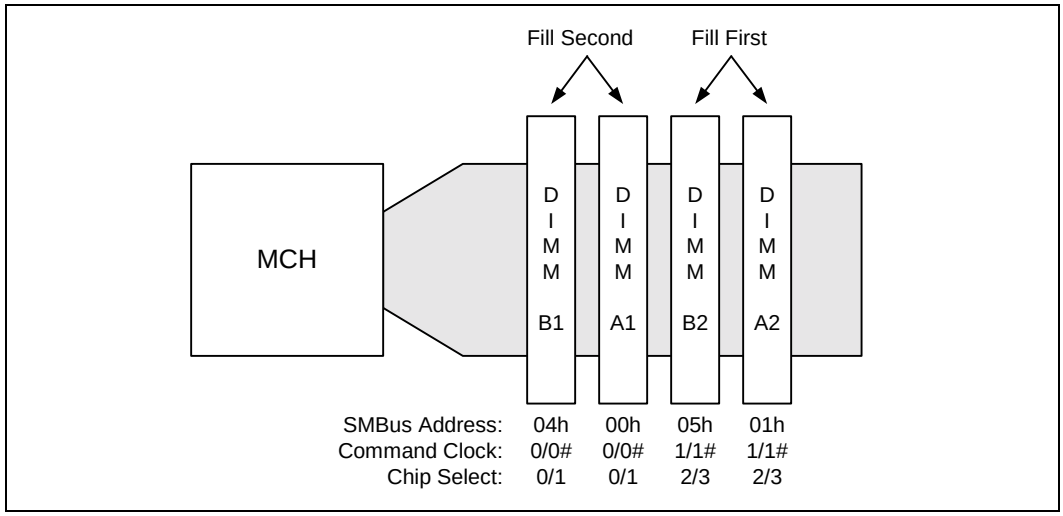


Figure 10. 2-DIMMs per Channel Implementation



3.2.1 Dual Channel Source Synchronous Signal Group Routing

Table 8 states the routing requirements for the DQ, DQS and CB signals. All signals in a data group must be length matched to the associated DQSs, as described in the *Intel® Xeon™ Processor and Intel® E7500/E7501 Chipset Compatible Platform Design Guide*. Length matching past the last DIMM connector is not critical. Route all data signals and their associated strobes on the same layer. Try to maintain routing the signals on the same layer. When a layer transition must occur, minimize the discontinuity in the ground reference plane. The source synchronous signals require series termination resistors (Rs) placed close to the first DIMM connector, and parallel termination resistors (Rtt) placed after the last DIMM connector. These solutions do not require DQS to CMDCLK pair length matching.

When resistor packs are used for the termination resistors, it is suggested that data group signals not be mixed with Source Clocked, Chip Select, or Clock Enable signals within the same resistor pack for purposes.

Table 8. Dual Channel Source Synchronous Signal Group Routing Guidelines

Parameter	1-DIMM Solution 0°[5], 25°[5], 90°	2-DIMM Solution 25°[5]	2-DIMM Solution 90°	Reference
Signal Group[2]	DQ[63:0], CB[7:0], DQS[17:0]			Note 6
Topology	Daisy Chain			
Reference Plane	Ground			
MCH to Rs Trace Impedance (Zo)	50 Ω ± 10%	50 Ω ± 10%	50 Ω ± 10%	
Rs to Rtt Trace Impedance (Zo)	50 Ω ± 10%	50 Ω ± 10%	50 Ω ± 10%	
MCH to Rs Trace Width	5 mils	5 mils	5 mils	
Rs to Rtt Trace Width	5 mils	5 mils	5 mils	
Nominal Trace Spacing	15 mils ± 1 mil	15 mils ± 1 mil	15 mils ± 1 mil	
MCH to DIMM1 Trace Length[3]	1.8" to 5.5"	1.8" to 4.5"	1.8" to 6.0"	
Rs to DIMM1 Trace Length	0.1" to 0.8"	0.1" to 0.8"	0.1" to 0.8"	
DIMM to DIMM Trace Length	Not Supported	1.8" to 2.2" ± 50 mil[4]	1.0" to 1.2" ± 50 mil[4]	
DIMM to Rtt Trace Length	< 0.8"	< 0.8"	< 0.8"	
Series Resistor (Rs)	10 Ω ± 2%	10 Ω ± 2%	10 Ω ± 2%	
Termination Resistor (Rtt)	39.2 Ω ± 1%	39.2 Ω ± 1%	39.2 Ω ± 1%	
MCH Breakout Guidelines	5/5, < 500 mils	5/5, < 500 mils	5/5, < 500 mils	
Length Tuning Requirements	DQ to DQS: ±25 mil[1]	DQ to DQS: ±25 mil[1]	DQ to DQS: ±25 mil[1]	

NOTES:

1. The DQS pair in the group must also be tuned to each other with this parameter. The DQ and DQS lines in the same group must be length tuned to all DIMMs. Tune all lengths to the Intel E7501 chipset MCH package trace lengths.
2. Route all data signals and their associated strobes on the same layer from MCH to Rtt.
3. The MCH to DIMM1 trace length is defined as Intel E7501 chipset MCH die pad (PCB trace velocity equivalent, see the *Intel® Xeon™ Processor and Intel® E7500/E7501 Chipset Compatible Platform Design Guide*) to DIMM1 pin.
4. Within the same group, this length range should not vary by more than 50 mils. However, the length may be anywhere from 1.0" to 1.2".
5. Ensure angled DIMM connector pin length differences are accounted for when tuning lengths.
6. See the *Intel® Xeon™ Processor and Intel® E7500/E7501 Chipset Compatible Platform Design Guide.*

3.2.2 Dual Channel Command Clock Routing

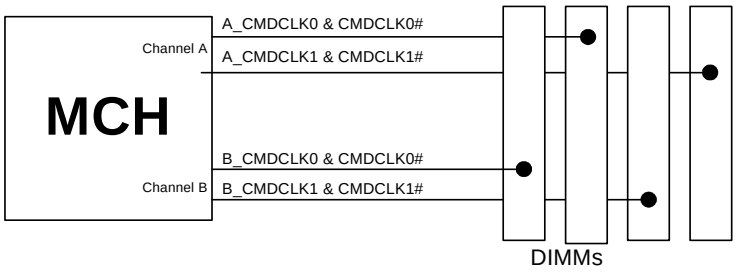
Only one differential clock pair is routed to each DIMM connector because the MCH only supports registered DDR DIMMs. All CMDCLK/CMDCLK# termination is on the DIMM modules. Route each clock and its compliment adjacent to each other. The two complimentary signals (e.g., CMDCLK0 and CMDCLK0#) must be length matched to each other within ± 2 mils and must be routed on the same layer. When a layer transition must occur, minimize the discontinuity in the ground reference plane.

Table 9. Dual Channel Command Clock Pair Routing Guidelines

Parameter	1-DIMM Solution 0°[1], 25°[1], 90°	2-DIMM Solution 25°[1]	2-DIMM Solution 90°	Reference
Signal Group	CMDCLK[3:0], CMDCLK[3:0]#			
Topology	Point to point			Figure 11
Reference Plane	Ground			Note 2
Differential Trace Impedance (Zo)	100 Ω ± 10%	100 Ω ± 10%	100 Ω ± 10%	
Nominal Trace Width	5 mils	5 mils	5 mils	
Differential Trace Spacing	7.5 mils	7.5 mils	7.5 mils	
Group Trace Spacing	20 mils	20 mils	20 mils	
MCH to DIMM1 Trace Length	3.0” to 4.0”	3.0” to 4.0”	3.0” to 4.0”	Figure 11
MCH to DIMM2 Trace Length	Not Supported	4.0” to 6.0”	4.0” to 6.0”	
MCH to DIMM3 Trace Length	Not Supported	Not Supported	Not Supported	
MCH to DIMM4 Trace Length	Not Supported	Not Supported	Not Supported	
MCH Breakout Guidelines	5/5, < 500 mils	5/5, < 500 mils	5/5, < 500 mils	
Length Tuning Requirements	CMDCLK to CMDCLK#: ± 2 mils	CMDCLK to CMDCLK#: ± 2 mils	CMDCLK to CMDCLK#: ± 2 mils	Figure 11

NOTES:
1. Ensure angled DIMM connector pin length differences are accounted for when tuning lengths.
2. See the *Intel® Xeon™ Processor and Intel® E7500/E7501 Chipset Compatible Platform Design Guide.*

Figure 11. Dual Channel 2-DIMM Command Clock Topology



NOTES:
1. CMDCLK/CMDCLK# must be matched to within ± 2 mils using package trace length compensation.
2. Unused CMDCLK/CMDCLK# pairs are no connects.
3. Indicated lengths measure from the MCH component pin to the DIMM connector pin.

3.2.3 Dual Channel Source Clocked Signal Group Routing

The MCH drives the command clock signals and the source-clocked signals together. That is, the MCH drives the command clock in the center of the valid window, and the source-clocked signals propagate with the command clock signal. Therefore, the critical timing is the difference between the command clock flight time and the source clocked signal flight time. The absolute flight time is not as critical.

When resistor packs are used for the termination resistors, it is suggested that data group signals not be mixed with Source Clocked, Chip Select, or Clock Enable signals within the same resistor pack for validation purposes.

Table 10. Dual Channel Source Clocked Signal Group Routing Guidelines

Parameter	1-DIMM Solution 0°, 25°, 90°	2-DIMM Solution 25°	2-DIMM Solution 90°	Reference
Signal Group[1,2]	RAS#, CAS#, WE#, MA[12:0], BA[1:0]			
Topology	Daisy Chain			Note 2
Reference Plane	Ground			
Trace Impedance (Zo)	50 Ω ± 10%	50 Ω ± 10%	50 Ω ± 10%	
Nominal Trace Width	5 mils	5 mils	5 mils	
Nominal Trace Spacing	15 mils	15 mils	15 mils	
MCH to DIMM1 Trace Length	1.8” to 5.5”	1.8” to 5.5”	1.8” to 5.5”	
DIMM to DIMM Trace Length	Not Applicable	1.8” to 2.2”	1.0” to 1.2”	
DIMM to Rtt Trace Length	< 0.8”	< 0.8”	< 0.8”	
Termination Resistor (Rtt)	39.2 Ω ± 1%	39.2 Ω ± 1%	39.2 Ω ± 1%	
MCH Breakout Guidelines	5/5, < 500 mils	5/5, < 500 mils	5/5, < 500 mils	

NOTES:
1. No length tuning required.
2. See the *Intel® Xeon™ Processor and Intel® E7500/E7501 Chipset Compatible Platform Design Guide.*

3.2.4 Dual Channel Chip Select Routing

The MCH provides eight chip select signals. Two chip selects must be routed to each DIMM (one for each side). Chip selects for each DIMM must be length matched to the corresponding clock within ± 875 mils and require parallel termination resistors (Rtt) to DDR VTERM.

Table 11. Dual Channel Chip Select Routing Guidelines

Parameter	1-DIMM Solution 0°, 25°, 90°	2-DIMM Solution 25°	2-DIMM Solution 90°	Reference
Signal Group[1,2]	CS[7:0]#			
Topology	Point to Point			Note 2
Reference Plane	Ground			
Trace Impedance (Zo)	50 Ω ± 10%	50 Ω ± 10%	50 Ω ± 10%	
Nominal Trace Width	5 mils	5 mils	5 mils	
Nominal Trace Spacing	15 mils	15 mils	15 mils	
MCH to DIMM1 Trace Length	3.0” to 4.0”	3.0” to 4.0”	3.0” to 4.0”	
MCH to DIMM2 Trace Length	Not Applicable	4.0” to 6.0”	4.0” to 6.0”	
MCH to DIMM3 Trace Length	Not Applicable	Not Applicable	Not Applicable	
MCH to DIMM4 Trace Length	Not Applicable	Not Applicable	Not Applicable	
Trace Length - DIMM to Rtt	0.3" to 1.5”	0.3" to 1.5”	0.3" to 1.5”	
Termination Resistor (Rtt)	39.2 Ω ± 1%	39.2 Ω ± 1%	39.2 Ω ± 1%	
MCH Breakout Guidelines	5/5, < 500 mils	5/5, < 500 mils	5/5, < 500 mils	

NOTES:
1. No length tuning required.
2. See the *Intel® Xeon™ Processor and Intel® E7500/E7501 Chipset Compatible Platform Design Guide.*

3.2.5 Dual Channel Clock Enable Routing

The MCH provides a single clock enable (CKE) signal. This signal is used during initialization to indicate that valid power and clocks are being applied to the DIMMs. Because the CKE signal has higher loading, it requires a lower impedance. The recommended impedance for the CKE signal is 40 Ω. This may be achieved using a 7.5 mils wide trace on the recommended stack-up (refer to the *Intel® Xeon™ Processor and Intel® E7500/E7501 Chipset Compatible Platform Design Guide).* It is acceptable to route the CKE signal 5 mils wide and 5 mils spacing when breaking out of the MCH. However, the trace must be widened to 7.5 mils before widening the spacing to 15 mils. The CKE signal requires a parallel termination resistor (Rtt) to DDR VTERM placed as close to the last DIMM connector as possible.

Table 12. Dual Channel Clock Enable Routing Guidelines

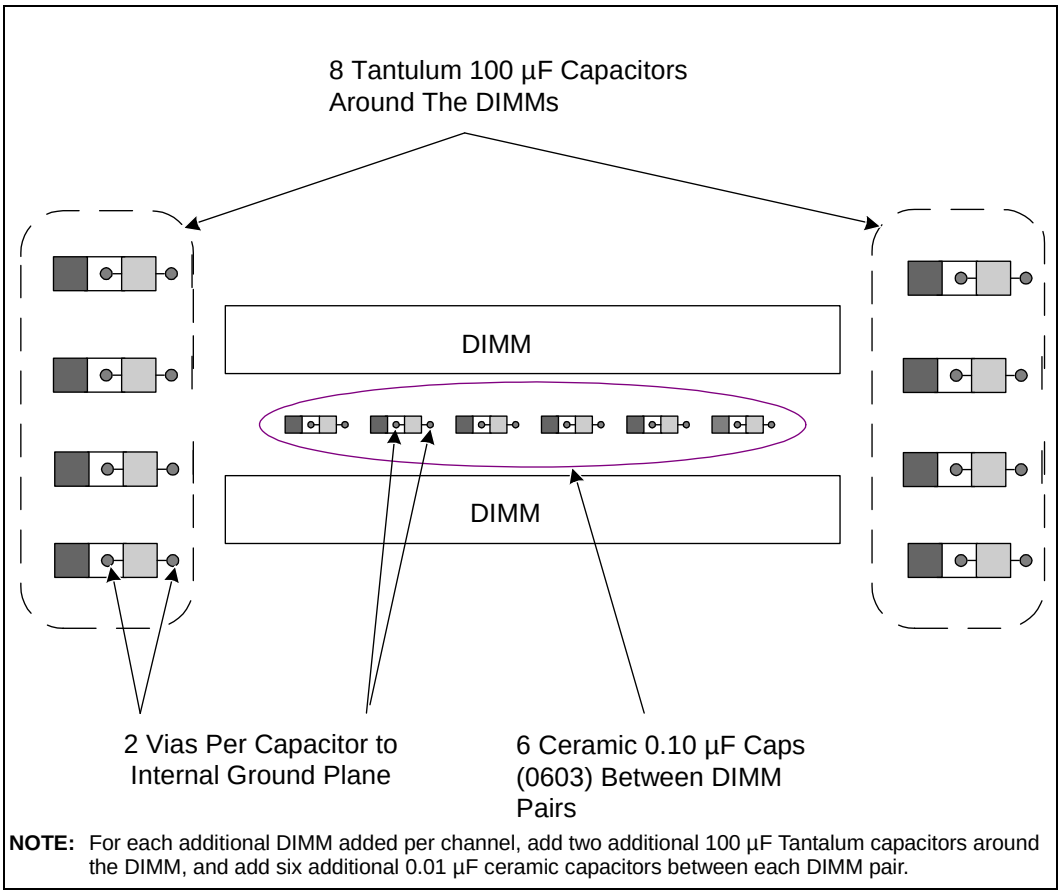
Parameter	1-DIMM Solution 0°, 25°, 90°	2-DIMM Solution 25°	2-DIMM Solution 90°	Reference
Signal Group[1,2]	CKE			
Topology	Daisy Chain with Stubs			Note 2
Reference Plane	Ground			
Trace Impedance (Zo)	40 Ω ± 10%	40 Ω ± 10%	40 Ω ± 10%	
Nominal Trace Width	7.5 mils	7.5 mils	7.5 mils	
Nominal Trace Spacing	15 mils	15 mils	15 mils	
MCH to DIMM1 Trace Length	1.8” to 6.0”	1.8” to 6.0”	1.8” to 6.0”	
DIMM to DIMM Trace Length	Not Applicable	1.8” to 2.2”	1.0” to 1.2”	
CKE Stub Trace Length	< 300 mils	< 300 mils	< 300 mils	
DIMM to Rtt Trace Length	< 0.8”	< 0.8”	< 0.8”	
Termination Resistor (Rtt)	39.2 Ω ± 1%	39.2 Ω ± 1%	39.2 Ω ± 1%	
MCH Breakout Guidelines	5/5, < 500 mils	5/5, < 500 mils	5/5, < 500 mils	

NOTES:
1. No length tuning required.
2. See the *Intel® Xeon™ Processor and Intel® E7500/E7501 Chipset Compatible Platform Design Guide.*

3.2.6 2.5 Volt Decoupling Requirements

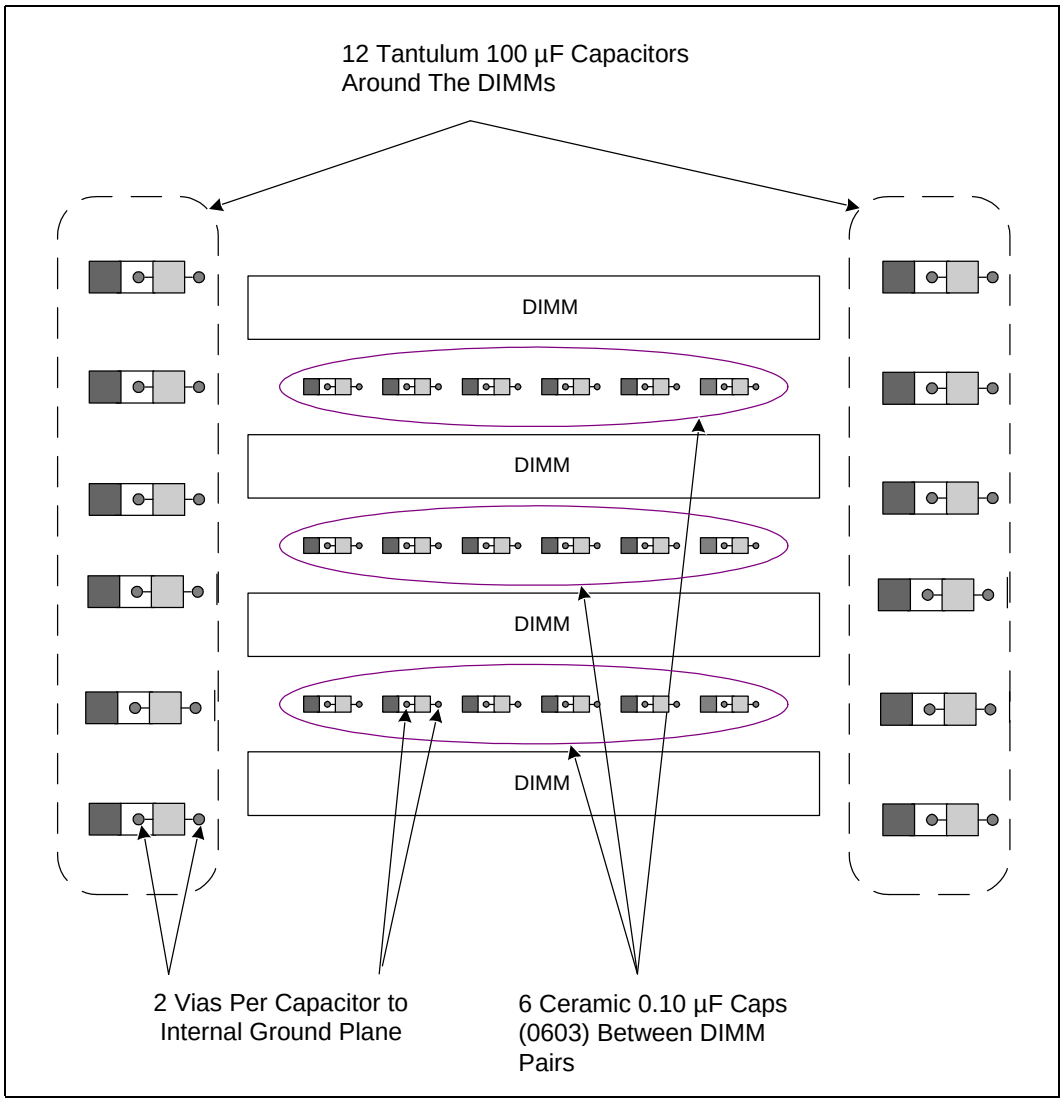
Decouple the DIMM connectors as shown in Figure 12 or Figure 13. Place six ceramic 0.1 µF (0603) capacitors between each pair of DIMM connectors. Place two Tantalum 100 µF capacitors around each DIMM connector and two additional Tantalum 100 µF capacitors per channel, keeping them within 0.5 inch of the DIMM connectors. Figure 12 depicts a 1-DIMM per channel decoupling scheme and Figure 13 depicts a 2-DIMM per channel decoupling scheme. When more DIMMs per channel may be used, continue the decoupling scheme for each additional DIMM connector.

Figure 12. 1-DIMM Per Channel Decoupling



NOTE: For each additional DIMM added per channel, add two additional 100 µF Tantalum capacitors around the DIMM, and add six additional 0.01 µF ceramic capacitors between each DIMM pair.

Figure 13. 2-DIMMs Per Channel Decoupling



3.3 Single Channel DDR Overview

In a single channel DDR configuration, channel A is the only channel that is active. Figure 14 and Figure 15 show channel A being routed to a single bank of DIMMs. The letter ‘A’ in the DIMM figure refers to the DIMM channel. The number following ‘A’ refers to the DIMM logical group.

The platform requires DDR DIMMs to be populated in-order, starting with the DIMM furthest from the MCH in a ‘fill-farthest’ approach (see Figure 14 and Figure 15). This recommendation is based on the signal integrity requirements of the DDR interface. Intel’s recommendation is to check for correct DIMM placement during BIOS initialization. Additionally, it is strongly recommended that all designs follow the DIMM ordering, SMBus Addressing, Command Clock routing and Chip Select routing documented in Figure 14 and Figure 15. This addressing must be maintained to be compliant with the reference BIOS code supplied by Intel.

Single Channel routing guidelines listed in the following sections are described for one or two DIMMs. When single channel three or four DIMMs guidelines are needed, follow the dual channel guidelines for three or four DIMMs listed in Section 3.2, “Dual Channel DDR Overview”.

Figure 14. Single Channel 2-DIMM Implementation

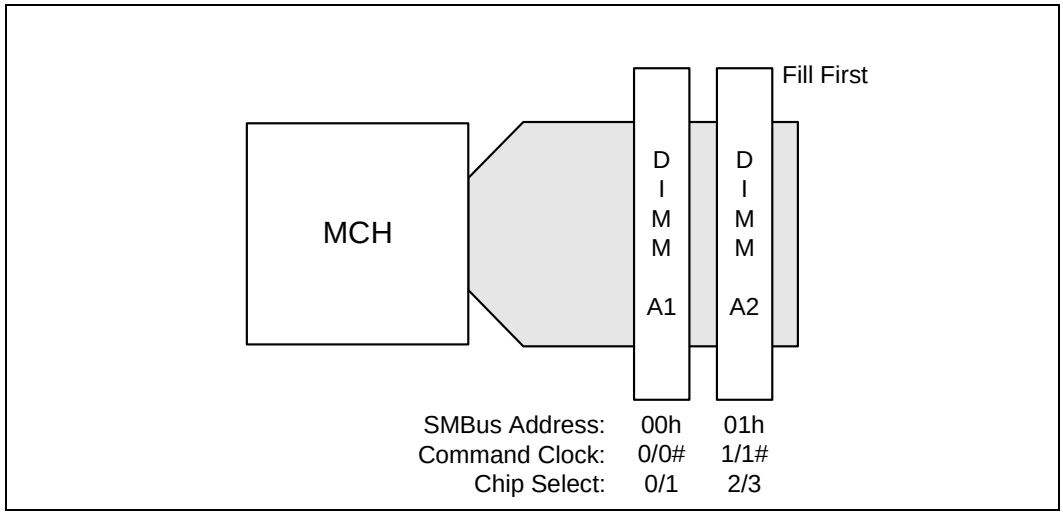
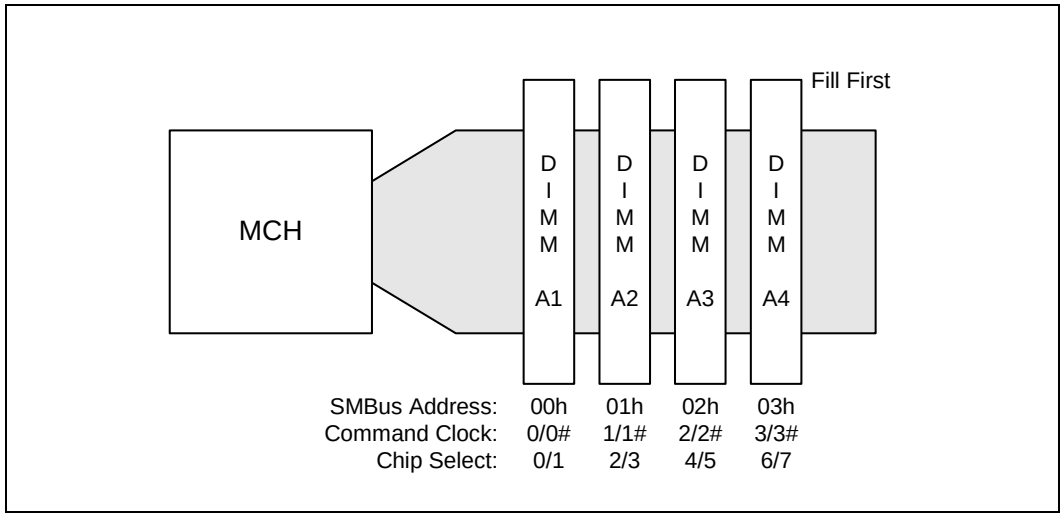


Figure 15. Single Channel 4-DIMM Implementation



3.3.1 Unused Channel B

Channel B is not used in a single-channel configuration. Therefore, Channel B’s associated signals should terminate as described in Table 13.

Table 13. Channel B Signal Terminations

Signal Name	Single Channel PCB Recommended Connection
Bidirectional Signal Group	
CB_B[7:0]	47 Ω +- 1% pullup to DDR Vterm (1.25 V). See Section 3.3.2.
DQ_B[63:0]	47 Ω +- 1% pullup to DDR Vterm (1.25 V). See Section 3.3.2.
DQS_B[17:0]	47 Ω +- 1% pullup to DDR Vterm (1.25 V). See Section 3.3.2.
RCVENOUT_B#	47 Ω pullup to DDR Vterm (1.25 V). See Section 3.3.7.1.
Output Signal Group	
CMDCLK_B[3:0] CMDCLK_B[3:0]#	No connect or connect each associated CMDCLK_Bx to CMDCLK_Bx# through a 120 Ω resistor.
MA_B[12:0] BA_B[1:0] RAS_B# CAS_B# WE_B# CS_B[7:0]# CKE_B[1:0]	No connect.
Input Signal Group	
DDRCOMP_B	24.9 Ω +-1% pull-down to Ground. See Section 3.3.7.2.
DRCVO_B	Connect to resistor divider network. See Section 3.3.7.4.
DDRVREF_B[3:0]	Connect to DDR VREF (1.25 V). See Section 3.3.7.3.

3.3.2 Single Channel Source Synchronous Signal Group Routing

The MCH source synchronous signals are divided into groups consisting of data bits (DQ) and check bits (CB). An associated strobe (DQS) exists for each DQ and CB group, as shown in Table 14. The MCH supports both x4 and x8 devices, and the number of signals in each data group depends on the type of devices that are populated. For example, when x4 devices are populated, the 72-bit channel is divided into 18 data groups (16 groups consisting of four data bits each, and two groups consisting of four check bits each). One DQS is associated with each of these groups (18 total). Likewise, when x8 devices are populated, the 72-bit channel is divided into a total of nine data groups. In this case, only nine of the 18 strobes are used.

Table 14. Single Channel DQ/CB to DQS Mapping

Data Group	Associated Strobe†
DQ[7:0]	DQS0, DQS9
DQ[15:8]	DQS1, DQS10
DQ[23:16]	DQS2, DQS11
DQ[31:24]	DQS3, DQS12
DQ[39:32]	DQS4, DQS13

† In x4 configurations, the high DQS is associated with the high nibble and the low DQS is associated with the low nibble. In x8 configurations, only the low DQS is used.

Table 14. Single Channel DQ/CB to DQS Mapping

Data Group	Associated Strobe†
DQ[47:40]	DQS5, DQS14
DQ[55:48]	DQS6, DQS15
DQ[63:56]	DQS7, DQS16
CB[7:0]	DQS8, DQS17

† In x4 configurations, the high DQS is associated with the high nibble and the low DQS is associated with the low nibble. In x8 configurations, only the low DQS is used.

Table 15 states the routing requirements for the DQ, DQS and CB signals. All signals in a data group must be length matched to the associated DQSs, as described in the *Intel® Xeon™ Processor and Intel® E7500/E7501 Chipset Compatible Platform Design Guide*. Length matching past the last DIMM connector is not critical. Route all data signals and their associated strobes on the same layer. Try to maintain routing the signals on the same layer. When a layer transition must occur, minimize the discontinuity in the ground reference plane. The source synchronous signals require series termination resistors (Rs) placed close to the first DIMM connector, and parallel termination resistors (Rtt) placed after the last DIMM connector. These solutions do not require DQS to CMDCLK pair length matching.

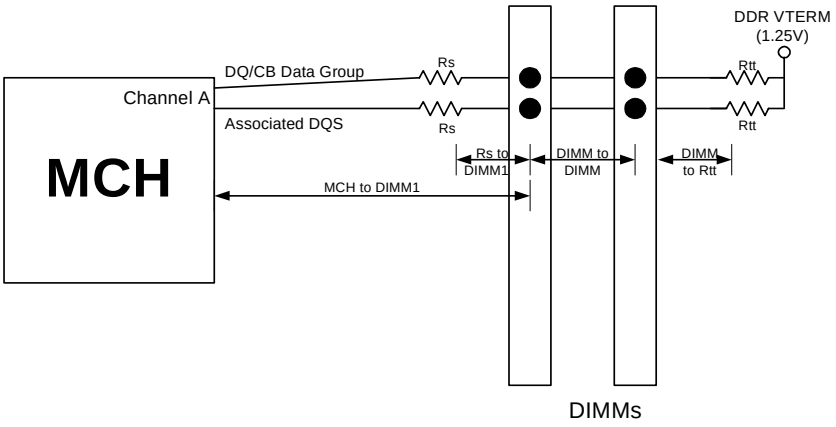
When resistor packs are used for the termination resistors, it is suggested that data group signals not be mixed with Source Clocked, Chip Select, or Clock Enable signals within the same resistor pack for validation purposes.

Table 15. Single Channel Source Synchronous Signal Group Routing Guidelines

Parameter	1-DIMM Solution 0°[5], 25°[5], 90°	2-DIMM Solution 25°[5]	2-DIMM Solution 90°	Reference
Signal Group[2]	DQ[63:0], CB[7:0], DQS[17:0]			
Topology	Daisy Chain			Figure 16
Reference Plane	Ground			
MCH to Rs Trace Impedance (Zo)	50 Ω ± 10%	50 Ω ± 10%	50 Ω ± 10%	Table 14
Rs to Rtt Trace Impedance (Zo)	50 Ω ± 10%	50 Ω ± 10%	50 Ω ± 10%	
MCH to Rs Trace Width	5 mils	5 mils	5 mils	Figure 16
Rs to Rtt Trace Width	5 mils	5 mils	5 mils	
Nominal Trace Spacing	15 mils ± 1 mil	15 mils ± 1 mil	15 mils ± 1 mil	
MCH to DIMM1 Trace Length[3]	1.8” to 5.5"	1.8” to 5.5"	1.8” to 6.0"	
Rs to DIMM1 Trace Length	0.1" to 0.8"	0.1" to 0.8"	0.1" to 0.8"	
DIMM to DIMM Trace Length	Not Supported	1.0” to 1.2” [4]	1.0” to 1.2” [4]	
DIMM to Rtt Trace Length	< 0.8”	< 0.8”	< 0.8”	
Series Resistor (Rs)	10 Ω ± 2%	10 Ω ± 2%	10 Ω ± 2%	
Termination Resistor (Rtt)	39.2 Ω ± 1%	39.2 Ω ± 1%	39.2 Ω ± 1%	
MCH Breakout Guidelines	5/5, < 500 mils	5/5, < 500 mils	5/5, < 500 mils	
Length Tuning Requirements	DQ to DQS: ± 25 mil[1]	DQ to DQS: ± 25 mil[1]	DQ to DQS: ± 25 mil[1]	Figure 17, Note 6

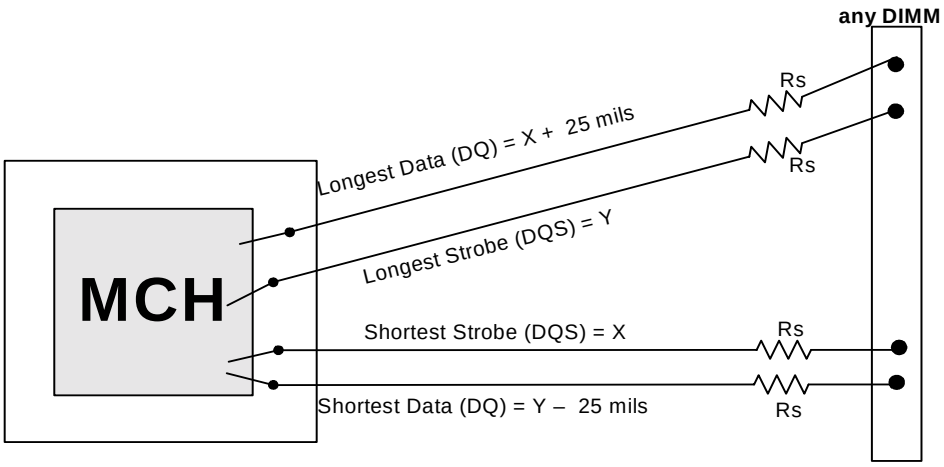
NOTES:
1. The DQS pair in the group must also be tuned to each other with this parameter. The DQ and DQS lines in the same group must be length tuned to all DIMMs. Tune all lengths to the Intel E7501 chipset MCH package trace lengths.
2. Route all data signals and their associated strobes on the same layer from MCH to Rtt.
3. The MCH to DIMM1 trace length is defined as Intel E7501 chipset MCH die pad (PCB trace velocity equivalent, see the *Intel® Xeon™ Processor and Intel® E7500/E7501 Chipset Compatible Platform Design Guide*)) to DIMM1 pin.
4. Within the same group, this length range should not vary by more than 50 mils. However, the length may be anywhere from 1.0” to 1.2”.
5. Ensure angled DIMM connector pin length differences are accounted for when tuning lengths.
6. See the *Intel® Xeon™ Processor and Intel® E7500/E7501 Chipset Compatible Platform Design Guide*.

Figure 16. Single Channel Source Synchronous Topology DIMM Solution



NOTE: Indicated lengths measure from the MCH component die pad (PCB trace velocity equivalent, see the *Intel® Xeon™ Processor and Intel® E7500/E7501 Chipset Compatible Platform Design Guide*) to the DIMM connector pin (including the series resistor).

Figure 17. Trace Length Matching Requirements for Single Channel Source Synchronous Routing



NOTES:

1. The DIMM displayed represents **any** DIMM. The two strobes must be within the same tolerance.
2. **All DIMMs must be length matched to the MCH within the specified tolerance.** A simple method to do this is to length match the DIMM to DIMM signals, then length match the MCH to the first DIMM within the specified tolerance.
3. There are eight Data lines (DQ) per group. For simplicity, only the longest and the shortest are represented here.
4. Indicated lengths measure from the MCH die pad to the DIMM connector pin (including the series resistor). The *Intel® Xeon™ Processor and Intel® E7500/E7501 Chipset Compatible Platform Design Guide* describes how to calculate the correct tuned lengths.
5. Rs only applies to the first DIMM in each channel.

3.3.3 Single Channel Command Clock Routing

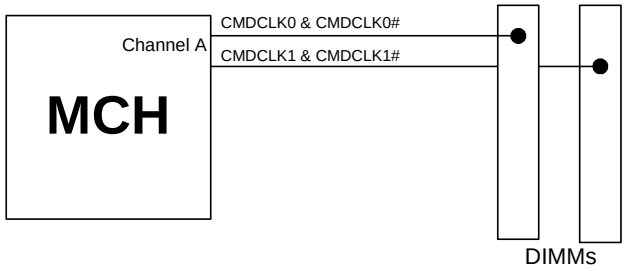
Only one differential clock pair is routed to each DIMM connector because the MCH only supports registered DDR DIMMs. All CMDCLK/CMDCLK# termination is on the DIMM modules. Route each clock and its compliment adjacent to each other. The two complimentary signals (e.g., CMDCLK0 and CMDCLK0#) must be length matched to each other within ± 2 mils and must be routed on the same layer. When a layer transition must occur, minimize the discontinuity in the ground reference plane.

Table 16. Single Channel Command Clock Pair Routing Guidelines

Parameter	1-DIMM Solution 0°[1], 25°[1], 90°[1]	2-DIMM Solution 25°[1]	2-DIMM Solution 90°	Reference
Signal Group[2]	CMDCLK[3:0], CMDCLK[3:0]#			
Topology	Point to point			Figure 18
Reference Plane	Ground			Figure 20
Differential Trace Impedance (Zo)	100 Ω ± 10%	100 Ω ± 10%	100 Ω ± 10%	
Nominal Trace Width	5 mils	5 mils	5 mils	
Differential Trace Spacing	7.5 mils	7.5 mils	7.5 mils	
Group Trace Spacing	20 mils	20 mils	20 mils	
MCH to DIMM1 Trace Length	3.0” to 4.0”	3.0” to 4.0”	3.0” to 4.0”	Figure 18
MCH to DIMM2 Trace Length	Not Supported	4.0” to 6.0”	4.0” to 6.0”	
MCH Breakout Guidelines	5/5, < 500 mils	5/5, < 500 mils	5/5, < 500 mils	
Length Tuning Requirements	CMDCLK to CMDCLK#: ± 2 mils	CMDCLK to CMDCLK#: ± 2 mils	CMDCLK to CMDCLK#: ± 2 mils	Figure 18

NOTES:
1. Ensure angled DIMM connector pin length differences are accounted for when tuning lengths.
2. See the *Intel® Xeon™ Processor and Intel® E7500/E7501 Chipset Compatible Platform Design Guide.*

Figure 18. Single Channel 2-DIMM Command Clock Topology



NOTES:
1. CMDCLK/CMDCLK# must be matched to within ± 2 mils using package trace length compensation.
2. Unused CMDCLK/CMDCLK# pairs are no connects.
3. Indicated lengths measure from the MCH component pin to the DIMM connector pin.

3.3.4 Single Channel Source Clocked Signal Group Routing

The MCH drives the command clock signals and the source-clocked signals together. That is, the MCH drives the command clock in the center of the valid window, and the source-clocked signals propagate with the command clock signal. Therefore, the critical timing is the difference between the command clock flight time and the source clocked signal flight time. The absolute flight time is not as critical.

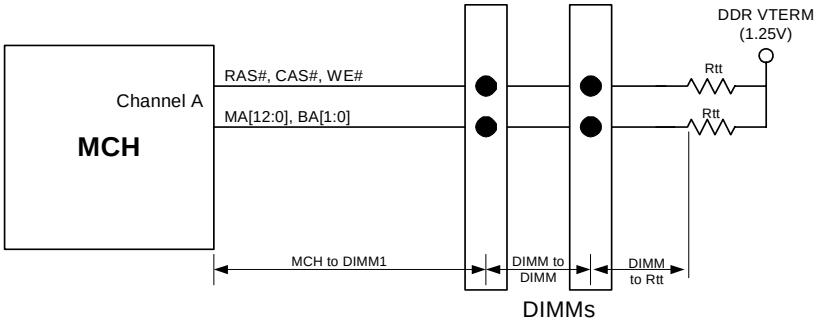
When resistor packs are used for the termination resistors, it is suggested that data group signals not be mixed with Source Clocked, Chip Select, or Clock Enable signals within the same resistor pack for validation purposes.

Table 17. Single Channel Source Clocked Signal Group Routing Guidelines

Parameter	1-DIMM Solution 0°, 25°, 90°	2-DIMM Solution 25°	2-DIMM Solution 90°	Reference
Signal Group[1,2]	RAS#, CAS#, WE#, MA[12:0], BA[1:0]			
Topology	Daisy Chain			Figure 19
Reference Plane	Ground			Figure 16
Trace Impedance (Zo)	50 Ω ± 10%	50 Ω ± 10%	50 Ω ± 10%	Note 2
Nominal Trace Width	5 mils	5 mils	5 mils	Figure 16
Nominal Trace Spacing	15 mils	15 mils	15 mils	Note 2
MCH to DIMM1 Trace Length	1.8” to 5.5”	1.8” to 5.5”	1.8” to 5.5”	Figure 19
DIMM to DIMM Trace Length	Not Applicable	1.0” to 2.2”	0.5” to 1.2”	
DIMM to Rtt Trace Length	< 0.8”	< 0.8”	< 0.8”	
Termination Resistor (Rtt)	39.2 Ω ± 1%	39.2 Ω ± 1%	39.2 Ω ± 1%	
MCH Breakout Guidelines	5/5, < 500 mils	5/5, < 500 mils	5/5, < 500 mils	

NOTES:
1. No length tuning required.
2. See the *Intel® Xeon™ Processor and Intel® E7500/E7501 Chipset Compatible Platform Design Guide*.

Figure 19. SIngle Channel Source Clocked Signal Topology



NOTE: Indicated lengths measure from the MCH component pin to the DIMM connector pin.

3.3.5 Single Channel Chip Select Routing

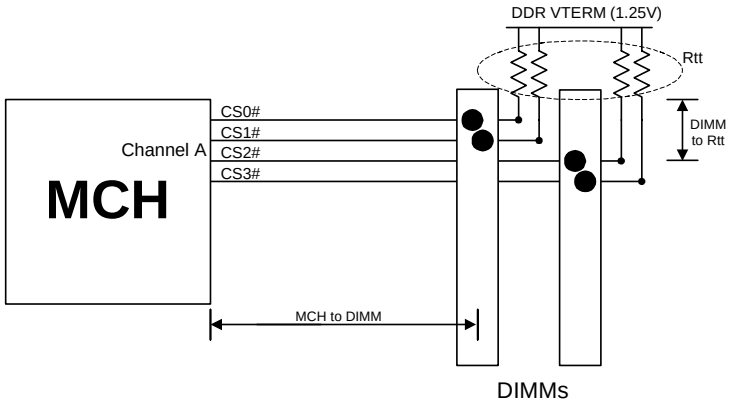
The MCH provides eight chip select signals. Two chip selects must be routed to each DIMM (one for each side). Chip selects for each DIMM must be length matched to the corresponding clock within ± 875 mils and require parallel termination resistors (Rtt) to DDR VTERM.

Table 18. Single Channel Chip Select Routing Guidelines

Parameter	1-DIMM Solution 0°, 25°, 90°	2-DIMM Solution 25°	2-DIMM Solution 90°	Reference
Signal Group[1,2]	CS[7:0]#			
Topology	Point to Point			Figure 20
Reference Plane	Ground			Figure 16
Trace Impedance (Zo)	50 Ω ± 10%	50 Ω ± 10%	50 Ω ± 10%	Note 2
Nominal Trace Width	5 mils	5 mils	5 mils	Figure 16
Nominal Trace Spacing	15 mils	15 mils	15 mils	
MCH to DIMM1 Trace Length	3.0” to 4.0”	3.0” to 4.0”	3.0” to 4.0”	Figure 20
MCH to DIMM2 Trace Length	Not Applicable	4.0” to 6.0”	4.0” to 6.0”	
Trace Length - DIMM to Rtt	0.3" to 1.5”	0.3" to 1.5”	0.3" to 1.5”	
Termination Resistor (Rtt)	39.2 Ω ± 1%	39.2 Ω ± 1%	39.2 Ω ± 1%	
MCH Breakout Guidelines	5/5, < 500 mils	5/5, < 500 mils	5/5, < 500 mils	

NOTES:
1. No length tuning required.
2. See the *Intel® Xeon™ Processor and Intel® E7500/E7501 Chipset Compatible Platform Design Guide*.

Figure 20. Single Channel Chip Select Topology



NOTES:
1. Unused CS*n*# signals are no connects.
2. Indicated lengths measure from the MCH component pin to the DIMM connector pin.

3.3.6 Single Channel Clock Enable Routing

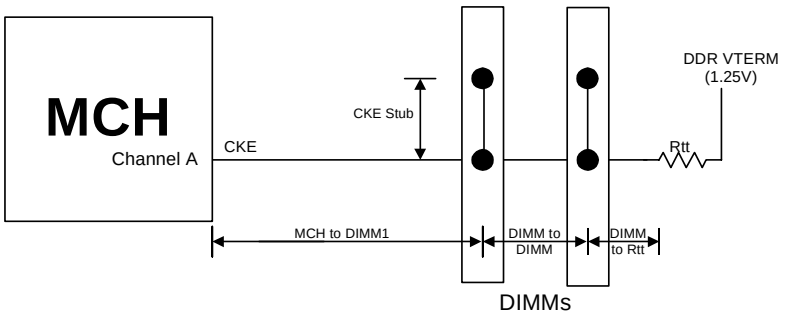
The MCH provides a single clock enable (CKE) signal. This signal is used during initialization to indicate that valid power and clocks are being applied to the DIMMs. Because the CKE signal has higher loading, it requires a lower impedance. The recommended impedance for the CKE signal is 40 Ω. This may be achieved using a 7.5-mils wide trace on the recommended stack-up (refer to Figure 16). It is acceptable to route the CKE signal 5 mils wide with 5 mils spacing when breaking out of the MCH. However, the trace must be widened to 7.5 mils before widening the spacing to 15 mils. The CKE signal requires a parallel termination resistor (Rtt) to DDR VTERM placed as close to the last DIMM connector as possible.

Table 19. Single Channel Clock Enable Routing Guidelines

Parameter	1-DIMM Solution 0°, 25°, 90°	2-DIMM Solution 25°	2-DIMM Solution 90°	Reference
Signal Group[1,2]	CKE			
Topology	Daisy Chain with Stubs			Figure 21
Reference Plane	Ground			Figure 16
Trace Impedance (Zo)	40 Ω ± 10%	40 Ω ± 10%	40 Ω ± 10%	Note 2
Nominal Trace Width	7.5 mils	7.5 mils	7.5 mils	Figure 16
Nominal Trace Spacing	15 mils	15 mils	15 mils	
MCH to DIMM1 Trace Length	1.8” to 6.0”	1.8” to 6.0”	1.8” to 6.0”	Figure 21
DIMM to DIMM Trace Length	Not Applicable	1.0” to 2.2”	0.50” to 1.2”	
CKE Stub Trace Length	< 300 mils	< 300 mils	< 300 mils	
DIMM to Rtt Trace Length	< 0.8”	< 0.8”	< 0.8”	
Termination Resistor (Rtt)	39.2 Ω ± 1%	39.2 Ω ± 1%	39.2 Ω ± 1%	
MCH Breakout Guidelines	5/5, < 500 mils	5/5, < 500 mils	5/5, < 500 mils	

NOTES:
1. No length tuning required.
2. See the *Intel® Xeon™ Processor and Intel® E7500/E7501 Chipset Compatible Platform Design Guide*.

Figure 21. Single Channel CKE Topology



NOTE: Indicated lengths measure from the MCH component pin to the DIMM connector pin.

3.3.7 Single Channel DC Biasing Signals

The DC Biasing signals are DDR signals which are not channel configuration specific. The following sections describe the DC Biasing signals.

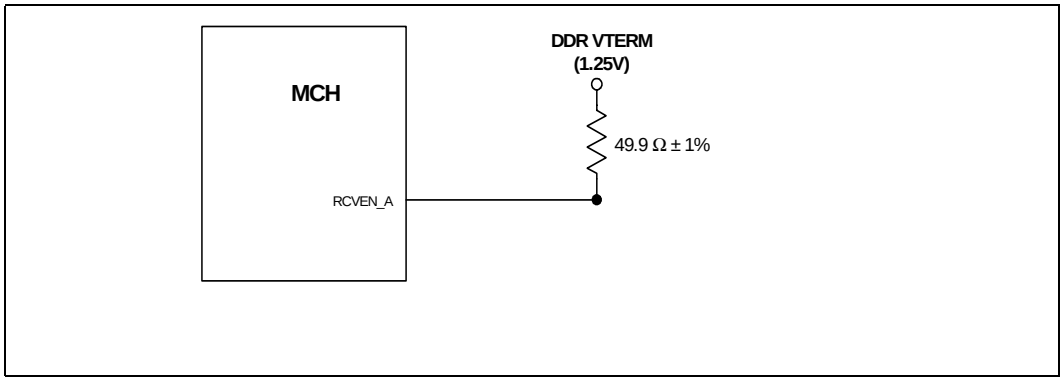
3.3.7.1 Single Channel Receive Enable Signal (RCVEN#)

The Intel E7501 chipset MCH requires a pull-up resistor (Rtt) to DDR VTERM on RCVEN. Table 20 lists the guidelines. Figure 22 summarizes these options.

Table 20. Single Channel Receive Enable Routing Guidelines

Parameter	Intel® E7501 Chipset MCH
Signal Group	Receive Enable
Topology	Pull-up
Trace Impedance (Zo)	50 Ω ± 10%
Nominal Trace Width	5 mils
Nominal Trace Spacing	15 mils
Trace Length - MCH RCVENIN to Rtt	No Requirement
Termination Resistor (Rtt)	49.9 Ω ± 1%
Total Length	No Requirement

Figure 22. Single Channel Receive Enable Signal Routing Guidelines



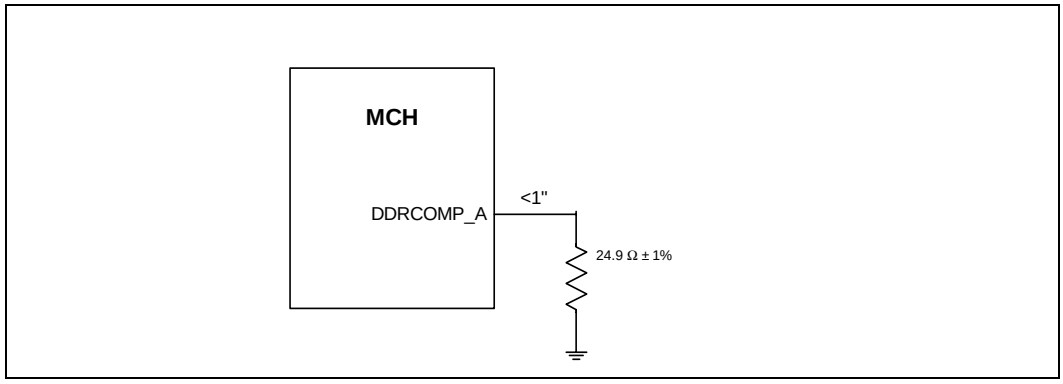
3.3.7.2 Single Channel DDRCOMP

The MCH uses DDRCOMP_A to calibrate the DDR channel buffers. This is periodically done by sampling the DDRCOMP pin on the MCH. The Intel E7501 chipset MCH calibrates using a 24.9 Ω ± 1% pull-down to ground. This may be implemented by routing a 15 mils wide trace to a resistive network as depicted in Figure 23. Place a decoupling capacitor between the pull-down and any other terminations.

Table 21. DDRCOMP Routing Guidelines

Parameter	Intel® E7501 Chipset MCH
Topology	pull-down
Nominal Trace Width	15 mils
Nominal Trace Spacing	20 mils
Trace Length - MCH to Rtt	< 1.0”
Termination Resistor (Rtt)	24.9 Ω ± 1%
Termination Voltage	Ground

Figure 23. Single Channel DDRCOMP Resistive Compensation



3.3.7.3 Single Channel DDRVREF and ODTCOMP

Follow design guidelines provided in the *Intel® Xeon™ Processor and Intel® E7500/E7501 Chipset Compatible Platform Design Guide*.

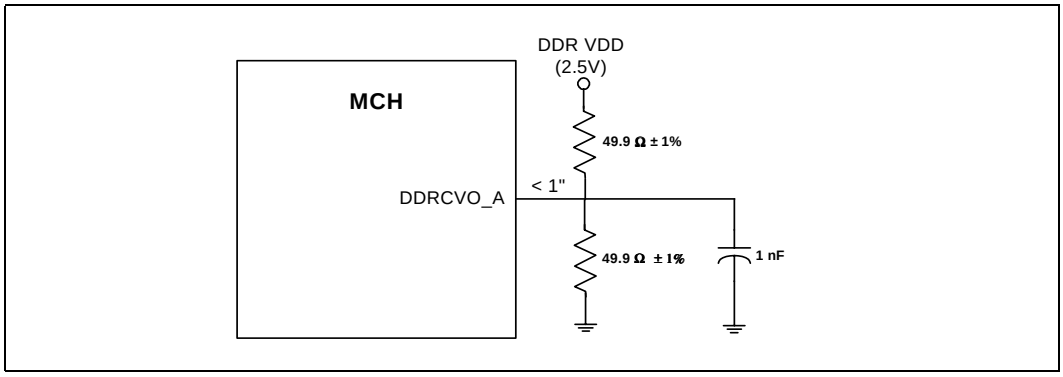
3.3.7.4 Single Channel DDRCVO

The MCH uses a compensation signal to adjust buffer characteristics and output voltage swing over temperature, process, and voltage skew. Calibration is done periodically by sampling the DDRCVO_A pins on the MCH. Place the voltage divider network (see Figure 24) within one inch of the MCH.

Table 22. DDRCVO Routing Guidelines

Parameter	Intel® E7501 Chipset MCH
Topology	Resistor Divider
Nominal Trace Width	15 mils
Nominal Trace Spacing	20 mils
Trace Length - MCH to Divider	< 1.0”

Figure 24. Single Channel DDRCVO Single Channel Routing Guidelines



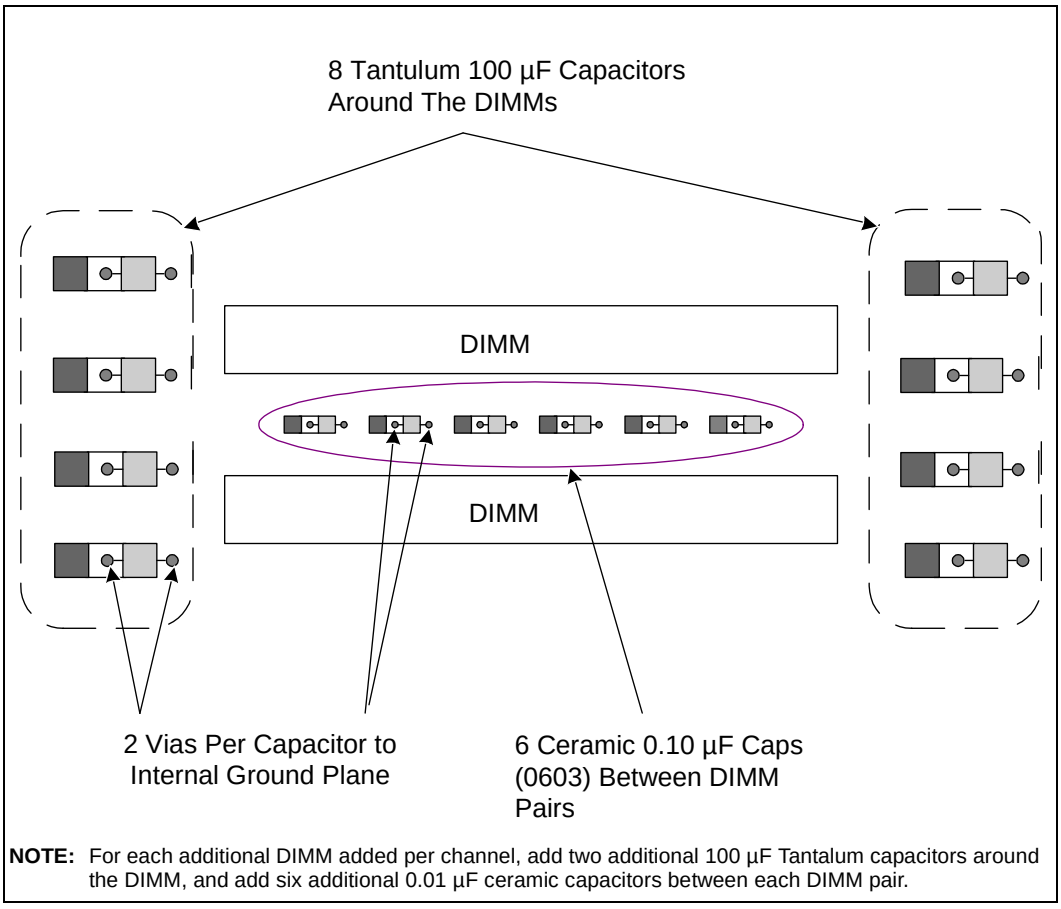
3.3.8 Single Channel DDR Signal Termination and Decoupling

Follow design guidelines provided in the *Intel® Xeon™ Processor and Intel® E7500/E7501 Chipset Compatible Platform Design Guide.*

3.3.9 2.5 V Decoupling Requirements

Decouple the DIMM connectors as shown in Figure 25 or Figure 26. Place six ceramic 0.1 µF (0603) capacitors between each pair of DIMM connectors. Place two Tantalum 100 µF capacitors around each DIMM connector and two additional Tantalum 100 µF capacitors per channel, keeping them within 0.5 inch of the DIMM connectors. Figure 25 depicts a single Channel 2-DIMM decoupling scheme and Figure 26 depicts a single channel 4-DIMM decoupling scheme.

Figure 25. Single Channel 2-DIMM Decoupling



NOTE: For each additional DIMM added per channel, add two additional 100 µF Tantalum capacitors around the DIMM, and add six additional 0.01 µF ceramic capacitors between each DIMM pair.

Figure 26. Single Channel 4-DIMM Decoupling